Manuel Monge

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Areas of Interests

Analog, mixed-signal, low-power circuits and systems. Biomedical and biologically inspired circuits and systems. Neuroscience and its synergy with electronics. Process variation correction. High-speed links.

Education

Ph.D.	**California Institute of Technology**, Pasadena, CA, USA Electrical Engineering, GPA: 3.9/4.0	Expected 2015
M.S.	**California Institute of Technology**, Pasadena, CA, USA Electrical Engineering, GPA: 3.9/4.0	Jun 2010
E.E.	**Pontifical Catholic University of Peru, PUCP**, Lima, Peru	Mar 2008
B.S.	**Pontifical Catholic University of Peru, PUCP**, Lima, Peru Electrical Engineering, *with honors*, GPA: 18.66/20	Feb 2008

Honors and Awards

- **2014 Rosen Scholar**,
  Rosen Bioengineering Center, California Institute of Technology, 2014
- **Third place winner of the Broadcom Foundation University Research Competition**,
  Broadcom, 2013
- **Atwood Fellowship**, *California Institute of Technology*, 2009
  Based on outstanding record of academic achievement.
- **Opportunity Grant (OG) Scholarship**, *U.S. Department of State's Bureau of ECA/A/S/A, administered by EducationUSA and Fulbright Commission in Peru*, Dec 2008
  Based on outstanding record of academic achievement.
- **Best Student Award**, *Pontifical Catholic University of Peru*, 2008
  Ranked first in the School of Science and Engineering, class of 2007-2.
- **Award of Research Initiation**, *Pontifical Catholic University of Peru*, 2007
  Based on academic achievement and research potential.
- **ERA-PUCP Fellowship**, *Pontifical Catholic University of Peru*, 2005-2007
  Received after ranked first in School of Science and Engineering during the first two years of studies.

Research Experience

California Institute of Technology

Research Assistant, Mixed-mode Integrated Circuits and Systems (MICS) group — Sep 2009-present
Advisor: *Prof. Azita Emami*

- **High-Density Fully Intraocular Self-Calibrating Retinal Prosthesis**
  - Designed and implemented a fully intraocular 1024-channel epiretinal prosthesis System-on-Chip (SoC) in 65nm CMOS technology
  - Self-calibrating digital scheme for precise current delivery
- **Minimally-Invasive Biological Interfaces**
  - In collaboration with *Prof. Mikhail Shapiro*
  - Study of techniques, approaches and opportunities for integrated circuits in biological interfaces using biophysical methods such as magnetic resonance, ultrasound and infrared light.
- **Wireless Chip-to-Chip Communication For Biomedical Applications**
  - Study of techniques, approaches and limitations of inductively coupled coils for low power data communication in multi-chip biomedical systems

- **Compressed-Sensing Signal Acquisition System**
  - Automated test system has been developed for measurements of the random modulator pre-integrator (RMPI) chip based compressed-sensing signal acquisition system
- **Data Generation for High-Speed Links**
  - Design of a high-speed cyclic register for an optical transmitter in 32nm SOI technology

Samsung Display America Laboratory (SDAL)

Summer intern, High-Speed Interfaces group — Jun 2013-Sep 2013
Advisor: *Amir Amirkhany, Ph.D., Principal Engineer, Manager of High-Speed Interfaces group*

- **On-Chip Channel Monitoring Circuits For High-Speed Data Links**
  - Design of a system for on-chip characterization of channel response, eye-diagram estimation and delay measurements. Design of a Phase Interpolator with LSB=2.6ps using state-of-the-art display technology.

Pontifical Catholic University of Peru

Research Assistant, Research Group in Microelectronics — Mar 2007-Aug2009
Advisor: *Prof. Carlos Silva Cardenas*

- Research on FPGA Digital Systems Design with VHDL.
- Senior Thesis: Design of a Multilayer Perceptron Neural Network on FPGA for character recognition

Publications

- S.Cerida, E.Raygada, C.Silva, M.Monge, **"A Low-Noise Fully Differential Recycling Folded Cascode Neural Amplifier"**, accepted to IEEE Latin American Symposium on Circuits and Systems, Feb. 2015
- L.Yue, M.Monge, M.Ozgur, S.Louie, C.Miller, A.Emami, M.Humayun, **"Simulation and measurement of transcranial near infrared light penetration"**, accepted to SPIE Photonics West, Feb. 2015
- *(Invited paper)* M.Monge and A.Emami, **"Design Considerations for High-Density Fully Intraocular Epiretinal Prostheses"**, IEEE Biomedical Circuits and Systems Conference (BioCAS), Oct 2014
- *(Invited paper)* M.Monge, M.Raj, M.Honarvar-Nazari, H.C.Chang, Y.Zhao, J.Weiland, M.Humayun, Y.C.Tai, A.Emami, **"A Fully Intraocular High-Density Self-Calibrating Epiretinal Prosthesis"**, IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), vol.7, no.6, pp.747-760, Dec 2013
- M.Monge, M.Raj, M.Honarvar-Nazari, H.C.Chang, Y.Zhao, J.Weiland, M.Humayun, Y.C.Tai, A.Emami-Neyestanak, **"A Fully Intraocular 0.0169mm^2/pixel 512-Channel Self-Calibrating Epiretinal Prosthesis in 65nm CMOS"**, IEEE International Solid-State Circuits Conference (ISSCC), Feb 2013
- J. Chang, Y. Liu, D. Kang, M. Monge, Y. Zhao, C.C. Yu, A. Emami-Neyestanak, J. Weiland, M. Humayun, Y.C. Tai, **"Packaging Study for a 512-Channel Intraocular Epiretinal Implant"**, IEEE International Conference on Micro Electro Mechanical Systems(MEMS), Jan. 2013
- J.Yoo, S.Becker, M.Loh, M.Monge, E.Candes, A.Emami-Neyestanak, **"A 100MHz-2GHz 12.5x sub-Nyquist Rate Receiver in 90nm CMOS"**, IEEE RFIC Symposium, Jun 2012
- J.Yoo, S.Becker, M.Loh, M.Monge, E.Candes, A.Emami-Neyestanak, **"Design and Implementation of a fully integrated Compressed-Sensing Signal Acquisition System"**, IEEE ICASSP, Mar 2012
- W.Bartra, M.Monge, C.Silva, R.Reis, **"Physical synthesis of an n-bits pipelined Division Module"**, XVI Workshop Iberchip, Iguacu Falls, Brasil, Feb 2010
- M. Monge, M. Raffo, C. Silva, **"Design of an architecture for a Multilayer Perceptron Neural Network on FPGA"**, XIV Workshop Iberchip, Puebla-México, Feb 2008

Talks and Presentations

- **"Integrated Circuits for Implantable Medical Devices"**, National University of Engineering

(UNI), Peru, December 17, 2014
- **"High-Density Fully Intraocular Epiretinal Prostheses"**, Medical Engineering Industry Day Poster Session, California Institute of Technology, October 29-30, 2014
- **"Fully Intraocular 512-Channel Self-Calibrating Epiretinal Prosthesis"**, Broadcom Foundation University Research Competition (BFURC), June 05-06, 2013
- (Invitated Talk) **"Biomedical Integrated Circuits: Neural Prostheses and Bio-sensors"**, Pontifical Catholic University of Peru (PUCP), March 08, 2013
- (Invitated Talk) **"Biomedical Integrated Circuits: Neural Prostheses and Bio-sensors"**, Cayetano Heredia Peruvian University (UPCH), March 14, 2013
- **"A 65nm CMOS Retinal Prosthesis IC"**, Biomimetic MicroElectronic Systems Engineering Research Center (BMES-ERC), Center-wide and Industrial Advisory Board Meeting, March 28-29, 2012
- **"A 1024-Channel Neurostimulator SoC in 65nm CMOS for Intraocular Retinal Prosthesis"**, BMES-ERC, Annual Site Visit, June 15-16, 2011

Teaching Experience

California Institute of Technology

Co-Mentor, EE 80 abc Senior Thesis — Sep-Jun 2012
- Mentored: Angie Wang, now graduate student at UC Berkeley
- Thesis: Test System and External Circuitry of a Retinal Prosthesis

Co-Mentor, Summer Undergraduate Research Fellowship (SURF) — Jun-Sep 2012
- Mentored: Julie Jester, Kirk and Marjory Dawson Family SURF Fellow
- Project: Retinal Prosthesis System for Vision Restoration

Co-Mentor, Summer Undergraduate Research Fellowship (SURF) — Jun-Sep 2012
- Mentored: Angie Wang, Rose Hills Foundation SURF Fellow
- Project: Test System for a Retinal Prosthesis IC. **First Place**, Gee Family Poster Competition

Teaching Assistant, Department of Electrical Engineering — Jan 2012-Mar 2014
- *EE 124 Mixed-mode Integrated Circuits*, spring 2012, spring 2013
- *EE 045 Electronics Laboratory*, winter 2012, winter 2013, winter 2014

National University of Trujillo, Peru

Instructor, Department of Mechanical Engineering — Aug 2009
- *Digital Electronic Laboratory 1*

Pontifical Catholic University of Peru

Instructor, Department of Electrical Engineering — Mar 2008-Dec 2014
- *Senior Thesis*, spring-fall 2013, fall 2014
- *Digital Circuits Laboratory*, spring-fall 2008, spring 2009

Teaching Assistant, Dept. of Electrical Eng. and Telecom. Eng — Mar 2008-Jul 2009
- *Digital Circuits*, fall 2006, spring-fall 2007, spring-fall 2008, spring 2009
- *Microelectronics, Computer Architecture*, fall 2008
- *Digital Electronics*, spring-fall 2007, spring 2008
- *Digital Systems*, spring 2008
- *Communications Theory 1*, fall 2007, spring 2008
- *Electronic Design 2, Electrical Systems Laboratory*, fall 2007
- *Electrical Circuits*, fall 2006

Skills

- **Languages:** Verilog, VHDL, SPICE/Spectre, C
- **Software:** Virtuoso, Encounter, Design Compiler, Calibre, Matlab/Simulink, Quartus II, ISE

Personal and Professional Activities

- Ad hoc reviewer, IEEE Transactions on Biomedical Circuits and Systems (TBIOCAS)
- IEEE Graduate Student member

- IEEE Solid-State Circuits Society (SSCS) member
- IEEE Circuits and Systems Society (CASS) member
- SURF seminar judge for oral presentation competition, Caltech, 2011-2012
- Student Leader, International Student Programs (ISP), Caltech, 2011-present
- Student Representative, Pontifical Catholic University of Peru, 2004-2005
- Peruvian National Swim Team, 2000, 2001